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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER

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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 2/95)

1- File Copy

Office Action Summary

Application No.	Applicant(s)
09/362,200	Nakazato Et.al.
Examiner	**Art Unit**
Edgardo Ortiz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 25, 2001*.

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-34 and 39-47* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-34 and 39-47* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 3

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

This Office Action is in response to an election filed July 25, 2001 on which Applicant elected Group I (Claims 1-34 and 39-47).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

Claims 1-7, 9, 10, 12-21, 23-34 and 40-47 are rejected under 35 § U.S.C. 102 (e) as being anticipated by Chang et.al. (U.S. Patent No. 5,619,052). With regard to Claim 1, Chang teaches a memory device having a lamination structure including an insulating film (14) and a semiconductor film (18), the lamination structure being disposed between an electrode structure (20) and a charge storing node, the lamination structure having an energy band profile that changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing between the electrode structure and the change storing node in the second configuration. See Figure 1.

With regard to Claim 2, Chang teaches a memory device having a control electrode (20), the energy band profile being changed between the first and the second configuration in response to a voltage supplied to the control electrode.

With regard to Claim 3, Chang teaches a path for carrier carriers (channel), a charge storing node to produce a filed which alters a conductivity of the path, a lamination structure including an insulating film (14) and a semiconductor film (18), the lamination structure being disposed between an electrode structure (20) and the charge storing node, the lamination structure having an energy band profile that changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing between the electrode structure and the change storing node in the second configuration. See Figure 1.

With regard to Claim 4, Chang teaches a memory device having a control electrode (20), the energy band profile being changed between the first and the second configuration in response to a voltage supplied to the control electrode.

With regard to Claim 5, Chang teaches a source-drain path for carrier carriers (channel), a charge storing node to produce a filed which alters a conductivity of the path, a lamination structure including an insulating film (14) and a semiconductor film (18), the lamination structure being

disposed between an electrode structure (20) and the charge storing node, the lamination structure having an energy band profile that changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing between the electrode structure and the change storing node in the second configuration. See Figure 1.

With regard to Claim 6, Chang teaches a memory device having a control electrode (20), the energy band profile being changed between the first and the second configuration in response to a voltage supplied to the control electrode.

With regard to Claim 7, Chang teaches an insulating film (14) and a conductive film (18) are formed of silicon nitride and silicon material respectively.

With regard to Claim 9, Chang teaches a lamination structure further including another film of silicon material (16), the silicon nitride film (14) being disposed between the film of silicon material (18) and the other film of silicon material (16).

With regard to Claim 10, Chang teaches a semiconductor film (18) with a silicon material comprising polysilicon.

With regard to Claim 12, Chang teaches a semiconductor film (18) with a silicon material comprising polysilicon.

With regard to Claim 13, Chang teaches a lamination structure including an insulating film (14) and a electrically conductive film (18), the lamination structure being disposed between a first terminal and a second terminal, the lamination structure having an energy band profile that changeable between a first configuration in which a barrier height of the energy band profile is high and a second configuration in which the barrier height of the energy band profile is low, an electric current flowing between the electrode structure and the change storing node in the second configuration. See Figure 1.

With regard to Claim 14, Chang teaches a memory device having a control electrode (20), the energy band profile being changed between the first and the second configuration in response to a voltage supplied to the control electrode.

With regard to Claim 15, Chang teaches a charge storage node, an electrode structure (20) and a barrier structure between the electrode structure and the charge storage node, the barrier structure providing a variable internal electrostatic barrier potential configurable by an external bias to provide selectively a relatively low barrier height for which charge carriers can pass

between the electrode structure and the charge storage node and a relatively high barrier height to store charge carriers on the charge storage node. See Figure 1.

With regard to Claim 16, Chang teaches a barrier structure includes a region of barrier material (14) providing a barrier component which is narrower and higher than that provided by the internal electrostatic barrier potential.

With regard to Claim 17, Chang teaches a height of said barrier component (14) raised and lowered in response to raising and lowering of the height of the barrier provided by the variable internal electrostatic barrier potential.

With regard to Claim 18, Chang teaches a barrier material formed from a material selected from the group consisting of silicon dioxide and silicon nitride.

With regard to Claim 19, Chang teaches a barrier structure includes a region of barrier material (14) providing a barrier component which is narrower and higher than that provided by the internal electrostatic barrier potential.

With regard to Claim 20, Chang teaches a gate (20) to receive external bias to configure the barrier between said high and low barrier heights.

With regard to Claim 21, Chang teaches a substrate (15), an array of memory cells (EEPROM) configured on the substrate and a plurality of word lines and data lines (76)extending between the cells, the word lines being operable to receive cell selection signals each of the memory cells comprising a charge storage node, an electrode (20) forming part of the data lines, and a barrier structure between the electrode and the charge storage node, the barrier structure providing a variable internal electrostatic barrier potential configurable selectively in response to an external bias provided by a selection signal applied to one of the word lines to provide a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node and a relatively high barrier height to store charge carriers on the charge storage node.

With regard to Claim 23, Chang teaches a barrier structure formed of crystalline material.

With regard to Claim 24, Chang teaches a barrier structure including polycrystalline silicon.

With regard to Claim 25, Chang teaches a gate electrode (20) to apply an external bias to the barrier structure.

With regard to Claim 26, Chnag teaches a substrate (15) configured so that the charge storage node is formed overlying the substrate, the barrier structure overlies the charge storage node and the electrode structure (20) overlies the barrier structure.

With regard to Claim 27, Chang teaches an insulating layer (17) overlying the substrate, the charge storage node, barrier structure and the electrode structure overlying the insulting layer.

With regard to Claim 28, Chang teaches further device features (11, 13) formed in the substrate (15) and underlying the insulating layer (17).

With regard to Claim 29, Chang teaches an insulating layer (17) comprising an oxide of the material of the substrate (15).

With regard to Claim 30, Chang teaches an insulating layer (17) extending over side edges of the barrier structure and the charge storage node.

With regard to Claim 31, Chang teaches a barrier structure substantially co-extensive with the charge storage node.

With regard to Claim 32, Chang teaches a barrier structure having a material composition that provides an internal relatively high internal electrostatic barrier in the absence of an applied voltage to the electrode structure, whereby the electrostatic barrier can be lowered upon application of the external bias to the electrode structure.

With regard to Claim 33, Chang teaches a gate (20) configured to apply external bias into the barrier structure selectively to control conduction of charge carriers between the electrode structure and the charge storage node.

With regard to Claim 34, Chang teaches a charge storage node made of conductive silicon material.

With regard to Claim 40, Chang teaches reading circuitry to read the level of charge stored on the charge storage nodes of the cells individually.

With regard to Claim 41, Chang teaches writing circuitry to write charge to the charge storage nodes of the cells individually.

With regard to Claim 42, Chang teaches a barrier structure formed of crystalline material.

With regard to Claim 43, Chang teaches a barrier structure including polycrystalline silicon.

With regard to Claim 44, Chang teaches a gate electrode (20) to apply an external bias to the barrier structure.

With regard to Claim 45, Chang teaches a substrate (15), an array of memory cells (EEPROM) configured on the substrate and a plurality of word lines and data lines (76)extending between the cells, the word lines being operable to receive cell selection signals each of the memory cells comprising a charge storage node, an electrode (20) forming part of the data lines, and a barrier structure between the electrode and the charge storage node, the barrier structure providing a variable internal electrostatic barrier potential configurable selectively in response to an external bias provided by a selection signal applied to one of the word lines to provide a relatively low barrier height for which charge carriers can pass between the electrode structure and the charge storage node and a relatively high barrier height to store charge carriers on the charge storage node, reading circuitry to read the level of charge stored on the charge storage nodes of the cells individually and writing circuitry to write charge to the charge storage nodes of the cells individually.

With regard to Claim 46, Chang teaches an electrically insulating layer (17) on a substrate (15) with an array of memory cells overlying the insulating layer.

With regard to Claim 47, Chang teaches a substrate comprising silicon, an insulating layer selected from a group comprising an oxide and a nitride of silicon, the charge storage node formed of a conductive silicon material and the barrier structure formed of polysilicon material.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8, 11, 22 and 39 are rejected under 35 § U.S.C. 103 (a) as being unpatentable over Chang et.al. (U.S. Patent No. 5,619,052). With regard to Claim 8, Chang, as stated supra, essentially discloses the claimed invention but fails to show, an additional film of silicon nitride in the lamination structure. It would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Chang to include an additional film of silicon nitride in the lamination structure, to prevent electrons to leak in to the control gate thus preventing leakage current.

With regard to Claim 11, which depends from claim 8, Chang teaches semiconductor material (18) comprising polysilicon.

With regard to Claim 22, a further difference between Chang and the claimed invention is, sense lines coupled to the source and refreshing circuitry to the sense lines to refresh data on the date lines. It would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Chang to include sense lines coupled to the source and refreshing circuitry to the sense lines to refresh data on the date lines, since it is a known practice in the art to include sense lines so that a voltage applied to the lines permits the reading of the memory cells and increase their threshold voltage.

With regard to Claim 39, a further difference between Chang and the claimed invention is, refreshing circuitry to refresh the level of charge stored in the charge storage node. It would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Chang to include a refreshing circuitry to increase the efficiency of reading and writing of the memory cells by conserving the charge stored in the node.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183. In case the Examiner can not be reached by a direct telephone call, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status

of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO / AU 2815

10/6/01

EDDIE LEE
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